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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known **Application Number** 09/782,687 **Filing Date** February 12, 2001 First Named Inventor Savoj, Jafar Art Unit 2633 **Examiner Name** Dalzid E. Singh

019717-001110US

Technology Center 2600

			U.S. PATENT D	OCUMENTS	ology ocinici
		Document Number			
Examiner	Cite No.1	Number Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
MC	· AA	US-4,535,459	08-13-1985	Hogge, Jr.	
MC	AB	US-5,301,196	04-15-1994	Ewen et al.	

FOREIGN PATENT DOCUMENTS

Attomey Docket Number

		Foreign Patent Document			Pages, Columns, Lines,		
Examiner Initials*	Cite No. ¹	Country Code ³ Number ⁴ Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Where Relevant Passages or Relevant Figures Appear		١,
	AC						
	AD						
		OTHER PRIOR ART NON PAT	ENT LITERATUI	RE DOCUMENTS			
Examiner Initials *	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
110	AE	C.R. HOGGE, JR., "A Self Correcting Clock Recovery Circuit", IEEE Journal of Lightwave Technology, vol. LT-3, no. 6, December 1985					
MC	AF	E. MULLNER, "A 20 Gb/s Parallel Phase Detector and Demultiplexer Circuit in a Production Silicon Bipolar Technology with fT=25 GHz", Proc. IEEE BCTM, pp. 43-45, Oct. 1996					
110	AG	M. RAU et al., *Clock/Data Recovery PLL Using Fno. 7, July 1997	lalf-Frequency Clock*	, IEEE Journal of Solid-Stat	e Circuits, vol. 32,		
10	АН	K. NAKAMURA et al., *A 6 Gb/s CMOS Phase De Symposium on VLSI Circuits Digest of Technical	etecting DEMUX Modu Papers	ule Using Half-Frequency C	lock", IEEE 1998		
1/0	Al	M. WURZER et al., *40-Gb/s Integrated Clock and BCTM 8.1, 1998	d Data Recovery Circu	uit in a Silicon Bipolar Techr	nology", IEEE		
ne	LA	JAFAR SAVOJ et al., "A 10-Gb/s CMOS Clock an Digest of Technical Papers	d Data Recovery Circ	uit*, IEEE 2000 Symposium	on VLSI Circuits		

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Examiner Signature	J Ellen Lum	Date Considered		3/03	

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¹ Unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.

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First Named Inventor Savoj, Jafar

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Examiner Name Dalzid E. Singh

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			U.S. PATENT DO	CUMENTS	
		Document Number			
Examiner	Cite No.1	Number Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
110	AA	US-6,121,804	09-19-2000	Bryan et al.	

			FOREIGN PA	TENT DOCUME	ENTS		
Examiner Initials*	Cite No.1	Foreign Patent Document			Name of Patentee or	Pages, Columns, Lines,	
		Country Code ³	Number ⁴ Kind Code ⁸ (if known)	Publication Date MM-DD-YYYY	Applicant of Cited Document	Where Relevant Passages or Relevant Figures Appear	T⁵
110	AB	PCT	WO 01/06696	01-25-2001	Chang et al.		
ne/	AC	PCT	WO 01/63767	08-30-2001	Green		

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